IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: JHA, et al.	§	Confirmation No.: 4721
	§	
	§	Group Art Unit: 2663
Serial No.: 10/731,632	§	
	§	Examiner: Rose, Kerri M.
Filed: December 9, 2003	§	
	§	Customer No.: 26290
For: Processing data for a TCP Connection Using an Offload Unit	§	
	§	

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PRE-APPEAL CONFERENCE BRIEF

In conjunction with the Pre-Appeal Brief Request for Review filed herewith, Applicant requests a Panel review of the Final Rejection in this matter (see the Final Office Action dated December 26, 2007). Although the remarks herein are focused on a specific factual issue raised by the rejection, nothing in this paper is meant to limit the scope of any arguments, either factual or legal, that Applicant may later present in a full appeal brief.

QUESTIONS FOR REVIEW

The Examiner has rejected pending claims 1-5, 8-12, 15-17, 19-25. Claims 1-5, 8-12, 15-17, 19-21 are rejected under 35 U.S.C. § 102(e) as anticipated by Hayes (U.S. 2003/0158906). Claims 22-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes. The Examiner's rejections are respectfully traversed. Specifically, Applicants disagree with the Examiner's position that Hayes teaches the limitations of a user buffer in a first portion of memory that is allocated to an application program and a legacy buffer in a second portion of the memory that is allocated to a software driver configured to communicate between an offload unit and a TCP stack.

ARGUMENTS SUBMITTED

Claims 1, 9, and 16 each recite limitations of a user buffer in a first portion of memory that is allocated to an application program and a legacy buffer in a second portion of the memory that is allocated to a software driver configured to communicate between an offload unit and a TCP stack. Hayes fails to teach or suggest these limitations.

In Figure 7, Hayes shows memory 108, but does not teach or suggest that a portion of memory 108 is allocated to a software driver and another portion of memory 108 is allocated to an application program. In fact, Hayes contains no description or suggestion that a portion of memory is allocated to a software driver and that a portion of memory is allocated to an application program.

The Examiner relies on a single sentence in Hayes describing the field of the invention, paragraph [0003], for the teachings of the claimed user buffer and legacy buffer. This sentence reads, "[m]ore particularly, one preferred embodiment of the invention enables the offloading auxiliary processor to deposit incoming user data directly into the user's memory space, bypassing the placing of a copy of the data into the operating system's memory...". In focusing on this sentence, the Examiner equates the incoming user data with the claimed frame, the user's memory space with the claimed first portion of memory that is allocated to the application program, and the operating system's memory with the claimed second portion of the memory that is allocated to the software driver configured to communicate between an offload unit and a TCP stack. However, neither the application program memory space nor the software driver's memory is illustrated in any of the Figures of Hayes or described in the specification. In fact, a careful reading of Hayes reveals that "user's memory space" and "operating system's memory" appear only in paragraph [0003] to describe the field of the invention. Therefore, the general statement of paragraph [0003] cannot rise to the level of a teaching required to anticipate or render obvious the pending claims.

Further, nowhere does Hayes specify where the user's memory space is located or to which function the user's memory space is allocated. As described in paragraph [0003] of Hayes, one purpose of the auxiliary processor is to reduce the memory bandwidth consumed relative to having the CPU perform protocol processing tasks.

Persons skilled in the art would recognize that, to accomplish such a purpose, the user's memory space would be located in NIC 26 of Figure 7 in order to reduce the memory bandwidth to memory 108 when NIC 26 offloads protocol processing tasks from CPU 28. With such an architecture, depositing user data in a memory in NIC 26 would reduce the memory bandwidth of memory 108. Such an architecture is completely in-line with the basic teachings of the Hayes reference, but this architecture does not satisfy the limitations of the pending claims. Again, the one sentence cited by the Examiner is simply too broad to conclude that it teaches or suggests the specific architecture covered by the pending claims.

In addition to failing to teach the claimed user buffers and legacy buffers, Hayes also fails to teach that frames are uploaded to those buffers. As noted by the Examiner, Figure 12 of Hayes illustrates the steps performed during the offloading process. According to Figure 12, portions of packets are passed through various drivers or to a default destination. Two of the drivers are located in offload host computer 12, and the remaining driver is located in NIC 26c (as shown in Figure 10). The default destination is not described at all in the Hayes reference. Hayes fails to describe any memory being associated with the various drivers or default destination. In paragraph [0060], Hayes describes that "device driver 114 strips away the Ethernet header and passes the IP packet to the IP protocol processor 116." Nowhere does Hayes teach or suggest a driver that stores data. Therefore, it is not reasonable to assume or conclude that device driver 114 would be associated with memory to store legacy buffers. Since Hayes fails to discuss the memories associated with the drivers or the default destination, Figure 12 cannot show that portions of the packets are uploaded to buffers in memory, as recited in the pending claims. Thus, for these additional reasons, Hayes does not teach or suggest the limitations recited in claims 1, 9, and 16 of the present application.

Regarding claim 21 of the present application, upon a thorough reading of Hayes, Applicant fails to find any teaching related to issuing an interrupt to the CPU, as recited in this claim. Again, Hayes has absolutely no disclosure relating to issuing an interrupt to the CPU. Therefore, Hayes cannot teach or suggest the limitations recited in claim 21.

Claims 22-25 recite the limitations of user buffers and legacy buffer that are stored in physically contiguous and non-contiguous memory locations. Again, Hayes is silent regarding the physical locations of buffers, and therefore Hayes fails to teach or suggest these limitations as well.

In the Advisory Action the Examiner stated that a reason is not provided by the Applicants to explain why the "software driver memory" is different from "operating system memory." The claim language is clear that the difference between the first portion of memory and the second portion of memory is that the first portion of memory is allocated to the application program and the second portion of memory is allocated to the software driver. The claim structure is squarely supported by Figures 2A and 2B of the present application which show that application memory space 227 and driver memory space 235 are different pieces of memory that both reside in system memory 130. In her response in the Advisory Action, the Examiner has incorrectly equated the application program with an operating system and has assumed that all of system memory is allocated to the operating system. Therefore, Applicants continue to take the position that the Examiner has incorrectly interpreted the claims and the teachings of the Hayes reference.

For the foregoing reasons, Applicants submit that Hayes fails to teach or suggest the limitations recited in independent claims 1, 9, and 16 and the claims dependent thereon. All of the claims currently pending in the application are therefore patentable over Hayes. In view of these clear distinctions, reconsideration and allowance of all the claims is respectfully requested.

Respectfully submitted,

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